520.37857CV3

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| Applicants: | K. KANETANI, et al. |
| Application No.: | Rule 1.53(b) Continuation of U.S. Patent Application Serial No. 10/230,295, filed August 29, 2002 |
| Filed: | On Even Date Herewith |
| For: | SEMICONDUCTOR INTEGRATED CIRCUIT AND SEMICONDUCTOR LOGIC CIRCUIT USED IN THE INTEGRATED CIRCUIT |
| Art Group of Parent: | 2819 |
| Examiner of Parent: | A. Q. Tran |

**PRELIMINARY AMENDMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 12, 2004

Sir:

Prior to examination, please amend the above-identified application as listed below and as set forth on the following pages:

**Amendments to the Specification; and**

**Remarks are included following the amendments.**